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OCTOBER 24-25, 2018

Holiday Inn Munich City Centre
Munich, Germany
DVCon-Europe.org
# Table of Contents

**General Chair’s Welcome** .................................................................................................................. 4

General Information ..................................................................................................................................... 6

Conference Floorplan ................................................................................................................................... 7

Steering Committee ...................................................................................................................................... 8

Technical Program Committee .................................................................................................................... 9

Conference Sponsor ................................................................................................................................... 10

About Accellera Systems Initiative ............................................................................................................ 10

**Conference Agenda** .......................................................................................................................... 12

Keynote Addresses: ................................................................................................................................... 13

Short Workshop: 1 ..................................................................................................................................... 14

Sponsored DV Tutorial: 1 ........................................................................................................................... 15

Sponsored ESL Tutorial: 1 .......................................................................................................................... 16

Short Workshop: 2 ..................................................................................................................................... 16

Short Workshop: 3 ..................................................................................................................................... 17

Sponsored DV Tutorial: 2 ........................................................................................................................... 18

Sponsored DV Tutorial: 3 ........................................................................................................................... 18

Short Workshop: 4 ..................................................................................................................................... 19

Session 1-2: .................................................................................................................................................. 19

Session 3-4: .................................................................................................................................................. 20

Poster Session: ............................................................................................................................................ 21

Keynote Address ......................................................................................................................................... 22

**DVCon Expo** ....................................................................................................................................... 23

Exhibitor Floorplan ..................................................................................................................................... 23

Exhibiting Companies ................................................................................................................................. 24

Exhibitor Listing........................................................................................................................................... 25
Dear friends,

Welcome to the 2nd Design and Verification Conference and Exhibition China (DVCon China).

Thanks to Accellera Systems Initiative, all the members of the DVCon China committee, and all community friends from the semiconductor industry and academy. DVCon China 2017 was the first DVCon held in China, and was a great success. Now DVCon China 2018 is here. This year, we have 3 keynotes from Cadence, Mentor and Synopsys, 4 tutorials from Accellera, Arm, Mentor and Synopsys, 2 short workshops from Mentor and Vtool, 8 technical papers, and dozens of poster papers covering Simulation, Emulation, Formal, HLS, Low Power, Portable Stimulus, UVM, Virtual Prototyping, Automobile, Big Data, and more.

As Dr. Wally Rhines, President and CEO of Mentor, a Siemens Business shared with us in the DVCon China 2017 opening keynote, Chinese engineers adapt new design and verification technologies faster worldwide. In this golden era for the China semiconductor industry, it's the pleasure of the DVCon China committee members to continue providing this platform of new design and verification methodologies, new technologies, new trends, and experience sharing to more Chinese IC engineers. Attendees can attend various technical sections covering different areas of Design and Verification, as well as visit the exhibition booths and communicate with the experts from different companies.

Thanks to the DVCon China 2018 committee members for all their hard work on DVCon China 2018.

Thanks to conference sponsors and Accellera Systems Initiative for their ongoing support of DVCon China, and to MP Associates for managing our conference program.

Special thanks to Andy Liu, David Cheng and Vincent Huang, the chairs of the DVCon China 2017 for their support of this year's DVCon China.

Friends, I look forward to seeing you at DVCon China 2018.

Sincerely yours,

Jinnan Huang
DVCon China 2018 General Chair
亲爱的朋友们，
我谨代表DVCon中国组委会欢迎您参加第二届DVCon中国暨第二届中国IC功能设计与验证大会。
感谢Accellera，组委会全体同仁，以及半导体业界伙伴们的支持，DVCon中国2017取得了巨大的成功。如今DVCon中国2018到来了。今年我们有由Accellera，ARM，Mentor和Synopsys提供的四个讲解教程(tutorial)，由Mentor和Vtool提供的两个短教程(short workshop)，八篇演讲技术论文，和大量的展板技术论文，涵盖了软件仿真，硬件仿真，形式验证，HLS，低功耗设计验证，Portable Stimulus，UVM，虚拟建模，汽车电子，大数据等领域。
Mentor, a Siemens Business 的董事局主席兼CEO，Wally Rhines博士，在DVCon中国2017的开场主题演讲中和我们分享的数据显示，在全球范围，中国的工程师能更快地接受并应用IC设计和验证的新技术和方法学。在这个中国半导体行业的黄金时代，DVCon中国组委会很荣幸地继续为大家提供这个平台来探讨IC设计和验证的新技术，新方法，新趋势，并为来自各个公司的专家交流分享经验创造机会。DVCon中国2018的参会者将能参与涵盖设计和验证的各个领域的深度主题演讲，访问参展商展位，和行业精英们交流。

感谢DVCon中国2018组委会的所有成员的共同努力和贡献。
感谢DVCon中国的赞助商和Accellera Systems Initiative对DVCon中国的持续支持，感谢MP Associates管理团队对会议筹备的支持。
特别感谢2017的DVCon中国的主席们Andy Liu，David Cheng和Vincent Huang对今年的DVCon中国的支持。
朋友们，欢迎参加DVCon中国2018。与你在上海相见，共创精彩的DVCon中国！
黄劲楠
DVCon中国2018主席
Registration Hours
Location: Foyer
Wednesday, April 18............................08:00-18:00 hours

Expo Hours
Location: Golden Ballroom Foyer
Wednesday, April 18............................10:00-19:30 hours

Parking Instructions
The DoubleTree by Hilton Shanghai Pudong has parking for DVCon China attendees. Self parking is 80 RMB for 24 hours. There are no in or out privileges.

DVCon Proceedings Distribution
DVCon China Conference Papers, Tutorial and Short Workshop presenter slides will be delivered electronically online via a username and password.
To Access: http://proceedings.dvcon-china.org
Username and password will be provided to registered conference attendees via email.

Wireless Information
Enjoy free Wi-Fi at DVCon China!
Connect to the complimentary hotel Wi-Fi with User Name: Hhonors-Meeting Password: Doubletree04

Attendee Coffee and Tea Breaks
Coffee and tea breaks will be offered at: 10:00-10:45 and 17:00-18:00

Social Media At DVCon
Follow DVCon China on WeChat and stay up to date on everything at DVCon China!
Awards Presentation

Wednesday, April 18 | Location: Ballroom AB | 18:00

Join us at 18:00PM in the Golden Ballroom for the announcement of the Best Paper and Best Poster Awards, before Keynote. Harry Foster from Mentor, A Siemens Business.

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Joe Xie
NVIDIA Corp.

Fan Yang
Fudan University

Fuzhen Yu
Intel Mobile Communication Xian Ltd.

David Zhang
Cadence Design Systems, Inc.

Landy Zhang
SZ DJI Technology Co., Ltd.
About Accellera Systems Initiative

Accellera Systems Initiative is an independent, not-for-profit organization dedicated to create, support, promote, and advance system-level design, modeling, and verification standards for use by the worldwide electronics industry. We are composed of a broad range of members that fully support the work of our technical committee to develop technology standards that are balanced, open, and benefit the worldwide electronics industry. Leading companies and semiconductor manufacturers around the world are using our electronic design automation (EDA) and intellectual property (IP) standards in a wide range of projects in numerous application areas to develop consumer, mobile, wireless, automotive, and other “smart” electronic devices. Through an ongoing partnership with the IEEE, standards and technical implementations developed by Accellera Systems Initiative are contributed to the IEEE for formal standardization and ongoing governance.

Our Mission

At Accellera our mission is to provide a platform in which the electronics industry can collaborate to innovate and deliver global standards that improve design and verification productivity for electronics products.

The purposes of the organization include:

• Provide design and verification standards required by systems, semiconductor, IP, and design tool companies to enhance a front-end design automation process.

• Collaborate with our community of companies, individuals, and organizations to deliver standards that lower the cost of designing commercial IC and EDA products and embedded system solutions, as well as increase the productivity of designers worldwide.

• Encourage availability and adoption of next-generation EDA and IP standards that encompass system-level, RT-level, and gate-level design flows.

• Collaborate with the electronic design community to deliver standards that increase designer productivity and lower the cost of product development.

• Provide mechanisms that enable the continued growth of the Accellera Systems Initiative user community including SystemC, Universal Verification Methodology (UVM), and IP-XACT.

• Standardize technical implementations developed by Accellera Systems Initiative through the IEEE.

Membership

Accellera members directly influence development of the most important and widely used standards in electronic design. Member companies protect and leverage their investment in design languages through their funding of a proven, effective and responsible organization. In addition, our members have a higher level of visibility in the EDA industry as active participants in Accellera-sponsored activities and as contributors to its decisions, which impact the EDA industry. For a full list of technical activities that are supported by Accellera, and for information on how to join us, please visit our website at www.accellera.org.

Accellera Systems Initiative Technical Excellence Award

Accellera wishes to recognize the outstanding achievements of its Working Group members by selecting outstanding contributors to our standards development process as recipients of the Accellera Systems Initiative Technical Excellence Award.

This annual award recognizes major contributions to the development of Accellera standards. Examples of such contributions may include leadership in standardization of new technologies, assuring achievement of standards development goals, and identifying opportunities to better serve the needs of the community through standards.

Any member of an Accellera Working Group is eligible for the award. Candidates can be nominated by Working Group chairs and are endorsed and selected by participants of the Accellera Technical Excellence Award Committee, which is a subcommittee of the Technical Committee.

Past Recipients:

2018: Richard Weber, Semifore
2017: Thomas Alsop, Intel
2016: Erwin de Kock, NXP
2015: Justin Refice, NVIDIA
2014: Andrew Goodrich, Cadence
2013: Janick Bergeron, Synopsys
2012: John Aynsley, Doulos

For more information about Accellera awards programs and to find out how to submit a nomination, visit accellera.org/about/awards.
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<table>
<thead>
<tr>
<th>Time</th>
<th>Event</th>
<th>Room</th>
<th>Sponsor</th>
</tr>
</thead>
<tbody>
<tr>
<td>08:45 - 09:00</td>
<td><strong>Opening Ceremony</strong></td>
<td>Ballroom AB</td>
<td></td>
</tr>
<tr>
<td>09:00 - 09:30</td>
<td><strong>Keynote: Industry’s Next Challenge: The Petacycle Challenge</strong></td>
<td>Ballroom AB</td>
<td>Synopsys</td>
</tr>
<tr>
<td>09:30 - 10:00</td>
<td><strong>Keynote: Smarter Verification – Beyond Brute Force</strong></td>
<td>Ballroom AB</td>
<td>Cadence</td>
</tr>
<tr>
<td>10:00 - 10:45</td>
<td><strong>Coffee and Tea Break</strong></td>
<td>Foyer</td>
<td></td>
</tr>
<tr>
<td>10:45 - 11:15</td>
<td><strong>Short Workshop 1:</strong> What Makes a Good Code Coverage Tool for HLS?</td>
<td>2A</td>
<td>Mentor</td>
</tr>
<tr>
<td>10:45 - 12:15</td>
<td><strong>DV Tutorial 1:</strong> Portable Test and Stimulus: The Next Level of Verification Productivity is Here</td>
<td>Ballroom A</td>
<td>Accellera</td>
</tr>
<tr>
<td>11:30 - 12:00</td>
<td><strong>Short Workshop 2:</strong> The Big Data Revolution Beautiful Servant or Dangerous Monster?</td>
<td>Ballroom B</td>
<td>Vtool</td>
</tr>
<tr>
<td>12:15 - 13:00</td>
<td><strong>Lunch</strong></td>
<td>Shanghai Spring</td>
<td></td>
</tr>
<tr>
<td>13:00 - 13:30</td>
<td><strong>Short Workshop 3:</strong> Using Mutation Coverage For Advanced Bug Hunting with Formal</td>
<td>2A</td>
<td>Mentor</td>
</tr>
<tr>
<td>13:00 - 14:30</td>
<td><strong>DV Tutorial 2:</strong> How to Stay Out of the News with ISO26262-Compliant Verification</td>
<td>Ballroom A</td>
<td>Mentor</td>
</tr>
<tr>
<td>13:45 - 14:15</td>
<td><strong>Short Workshop 4:</strong> Smart Verification: New Approach for FPGA Prototyping - Fast and Easy</td>
<td>2A</td>
<td>Cadence</td>
</tr>
<tr>
<td>14:45 - 15:45</td>
<td><strong>Session 1:</strong> Verification Methodology: Formal &amp; Emulator</td>
<td>Ballroom A</td>
<td></td>
</tr>
<tr>
<td>16:00 - 17:00</td>
<td><strong>Session 3:</strong> Memory Design and Verification</td>
<td>Ballroom A</td>
<td></td>
</tr>
<tr>
<td>17:00 - 18:00</td>
<td><strong>Coffee and Tea Break</strong></td>
<td>Foyer</td>
<td></td>
</tr>
<tr>
<td>17:00 - 18:00</td>
<td><strong>Poster Session:</strong></td>
<td>Foyer</td>
<td></td>
</tr>
<tr>
<td>18:00</td>
<td><strong>Award Presentation</strong></td>
<td>Ballroom AB</td>
<td>Mentor</td>
</tr>
<tr>
<td></td>
<td><strong>Keynote: The Next Big Thing in Design Driving the Next Big Wave in Verification</strong></td>
<td>Ballroom AB</td>
<td></td>
</tr>
</tbody>
</table>
Keynote: Industry's Next Challenge: The Petacycle Challenge

Time: 09:00 - 09:30 | Room: Ballroom AB

Speaker:
Chris Tice - Synopsys, Inc.

This keynote highlights how new growth segments, such as Automotive, IoT, Networking, 5G Mobile, etc. are fundamentally changing the requirements for verification. The keynote will emphasize how addressing the SoC verification, software bring-up and validation needed for these segments will change the nature of verification technologies and solutions.

Biography: Christopher Tice is vice president of Verification Continuum Solutions in the Verification Group, responsible for driving the growth of Synopsys’ verification business based on a foundation of solutions addressing fast-growing verticals such as automotive, networking, and IoT. Before joining Synopsys, he was an entrepreneur-in-residence at SK Telecom Innopartners. Mr. Tice spent 16 years at Cadence Design Systems where he was senior vice president and general manager of the Hardware and Systems Groups. Prior roles included vice president of Quickturn Design Systems and general manager of Weitek’s Processor Business Group. Mr. Tice received his BSEE with honors from the University of Florida and attended the MBA School at Florida Atlantic University. He was elected as an inaugural member of the Electrical and Computer Engineering Academy of the University of Florida in 2009.

Keynote: Smarter Verification – Beyond Brute Force

Time: 09:30 - 10:00 | Room: Ballroom AB

Speaker:
Michał Siwiński - Cadence Design Systems, Inc.

To optimize development schedules for advanced hardware/software developments, a combination of best in class engines for formal verification, simulation, emulation and FPGA based prototyping is required. Users are carefully optimizing the utilization of verification cycles executed on the various engines. Beyond brute force, beyond simply faster execution, a verification fabric offering verification management, debug, verification IP and portable stimulus for software driven SoC verification is poised to really increase “smartness” of verification and to guide users in their quest to best utilize every verification option they are given, in sequence and in combination. This keynote will introduce the latest trends driving the future of verification and provide a peak into the latest and upcoming improvements in efficient integration of the engines to increase verification productivity.

Biography: Michał Siwiński is the Vice President of Product Management and Operations for the System & Verification Group at Cadence Design Systems. His responsibilities include strategy, product portfolio & roadmap, business development, ecosystem and operations for the Cadence Verification Suite, delivery double-digit growth. The Suite includes JasperGold® formal verification, Xcelium™ parallel simulation, Palladium® emulation, and Protium™ FPGA prototyping core engines. Additionally, it includes Verification IP, Perspec™ tests, vManger™ metrics, and Indago™ debug as the multi-engine verification fabrics. Siwiński is also driving Cloud and Application-optimized verifications to address challenges faced by systems and semi companies across Mobile, Networking, Server, Consumer, IoT, Automotive, Aero & Defense, and other verticals, as part of the Cadence System Design Enablement strategy.

Previously at Cadence, Siwiński held various product management and product marketing positions, including responsibilities for functional verification, front-end digital, PCB & IC packaging, and starting the IP business. He also led the creation and deployment of key industry initiatives such the Universal Verification Methodology (UVM) from concept to industry standardization, establishing new verification technology sub-segments, and enabling the shift from point tools to integrated end-to-end verification platforms.

Siwiński joined Cadence via the acquisition of Verplex Systems, where he was responsible for the formal property checking product line, and held various roles in product and technical marketing, product engineering management, product validation, and field applications. Prior to Verplex, Siwiński performed digital design consulting services at Mentor Graphics, Inc.

Siwiński received his Bachelor of Science dual degree in Electrical Engineering and Computer Science from the University of California at Berkeley.
Exhibits

Time: 10:00 - 19:30 | Room: Foyer

Come to the DVCon China Expo and you will:
Meet vendors of design and verification tools, IP/VIP and services! Spend quality time with the vendors you most want to meet! Discover and learn about the latest products and services!

Short Workshop 1 - What Makes a Good Code Coverage Tool for HLS?

Time: 10:45 - 11:15 | Room: 2A

Organizer:
Mathilde Karsenti - Mentor, A Siemens Business

Closing code coverage in RTL is one of the toughest verification challenges and moving to High-Level Synthesis (HLS) hasn’t made coverage closure any easier. This workshop highlights the fundamental difference between closing coverage for software and HLS models, and how Catapult Coverage from Mentor, A Siemens Business lets you close RTL coverage on the HLS model.

Technology companies all around the world are successfully deploying HLS in their flows to reduce time to market and to cut down verification costs. The HLS-generated RTL though needs to fit into the well-established corporate verification flows. An important aspect of these flows is to close code coverage on the RTL. Traditionally, RTL designers have been using a mix of statement, branch, expression and functional coverage to guarantee the “goodness” of the RTL. To achieve all of this on machine-generated RTL is indeed a tall order. HLS users would love to have a flow where they close code coverage once on their high-level source code and use the same tests on the HLS-generated RTL to get close to 100% code coverage. That way, they can leverage the advantages of gcc simulation which is free and, at the same time, about 100X faster than RTL simulation. But are the conventional coverage tools up to this task or does covering a HLS model pose different challenges for coverage tools? Join this workshop for further insights.

Speaker:
Gagandeep Singh - Mentor, A Siemens Business

Thank you to our Sponsor:
DV Tutorial 1 - Portable Test and Stimulus: The Next Level of Verification Productivity is Here

**Time: 10:45 - 12:15 | Room: Ballroom A**

**Organizer:**
Tom Fitzpatrick - *Mentor, A Siemens Business*

Why reinvent the wheel? Up until now, verification teams had been unable to reuse tests as their efforts progressed from virtual platforms to RTL, block-level to system-level or from simulation to emulation, prototyping or silicon. The advent of UVM, constrained-random verification and functional coverage improved the reusability of portions of the verification environment, but these advances have not been able to enable reuse of verification intent throughout the product development process. Accellera formed the Portable Stimulus Working Group to produce a standard that would allow just this sort of verification intent reuse. This in-depth technical tutorial will focus on a set of typical design use-cases from a variety of applications and show how to use the Portable Test and Stimulus Standard to create an abstract model of your verification intent. The tutorial will then demonstrate how these models can be used to generate scenarios to be executed on the different platforms and environments used in your development process, and how the models can be reused and leveraged from project to project.

For each application, we will show:

- How to model the critical verification intent,
- How that model may be used to generate multiple compatible coverage-centered scenarios,
- How to map that intent into multiple target-specific implementations,
- How the declarative semantics of the model drive the generation of executable tests on different platforms to implement the desired scenarios.

**Speakers:**

- **Adnan Hamid** - Breker Verification Systems, Inc.
- **Sharon Rosenberg** - Cadence Design Systems, Inc.

Thank you to our Sponsor:
ESL Tutorial 1 - Leveraging Virtual Prototypes from Concept to Silicon

Time: 10:45 - 12:15 | Room: Ballroom B

Organizer:
Zheng Zhang - ARM Ltd.

This tutorial is targeting to describe ARM Models solutions regarding of Virtual Prototype technology. The tutorial will comprise three major parts: ARM Fast model for pre-silicon SW development, ARM Cycle model for System Exploration and Performance analysis, and Hybrid Virtual Prototyping for more use case like SW driven verification.

ARM Fast Models are accurate, flexible programmer’s view models of Arm IP, allowing you to develop software such as drivers, firmware, OS and applications prior to silicon availability. They allow full control over the simulation, including profiling, debug and trace. Fast Models can be exported to SystemC and TLM 2.0, allowing integration into the wider SoC design process. Fast Models are available for all Cortex processors, CCI and CCN interconnect, as well as other system IP. Fast Models are functionally accurate, so banked and co-processor registers, exception levels, translation tables and cache coherency are all available to programmers.

ARM Cycle models are compiled directly from Arm RTL and retain complete functional and cycle accuracy. This enables users to confidently make architectural decisions, optimize performance or develop bare metal software. Cycle Models are instrumented to enable detailed debug and analysis. CPU cores enable interactive debug with Arm DS-5. Additionally, all registers and PMUs are visible along with information related to cache hits, pipeline statistics and much more. Cycle Models are available 24 hours a day/7 days a week from Arm’s IP Exchange web portal. This portal enables users to access, configure, compile and manage their own models of Arm IP. Users are then emailed when their model is available for download.

Fast Model Hybrid simulation connect a CPU subsystem to peripherals on hardware emulators via AMBA transactors for emulation acceleration. Compatible with Cadence, Mentor Graphics and Synopsys emulators for maximum flexibility in your software development and IP validation process.

The tutorial will benefit not only existing System Level modeling like ESL users, but also show values for end user SW developers, architects, Verification engineers in IC design area.

Speaker:
Feng Niu - ARM Ltd.

Thank you to our Sponsor:

Short Workshop 2 - The Big Data Revolution Beautiful Servant or Dangerous Monster?

Time: 11:30 - 12:00 | Room: 2A

Chair:
Bin Liu - Intel Corp.

The world is experiencing the revolution of information, humanity shifting the hegemony from Science onto Data.

Cogita is a technological pathway that controls the data and creates measuring perceptions that do not forego or leave aside the human consciousness.

Cogita is a data screening, processing and visualization tool that targets ASIC and FPGA simulation based debug.

We explore a new way of simulation debug, by novel techniques of data processing. One of them consists of the human inherent talent to analyze reality by visualizing it. Others consist of sophisticated algorithms that help perform root cause analysis rapidly and efficiently.

Speakers and Author:
Dan Alexander, Hagai Arbel - VTool Ltd.
Anna M. Ravitzki - VTool Ltd.
Short Workshop 3 - Using Mutation Coverage For Advanced Bug Hunting with Formal

Time: 13:00 - 13:30 | Room: 2A

Organizer:
Sergio Marchese - OneSpin Solutions GmbH

Modern verification methodologies incorporate multiple coverage solutions. These range from functional to structural coverage, leverage various coverage models and operate using varied technologies in both the simulation and formal process. The main purpose of these coverage solutions is to establish a signoff metric that indicates when enough verification has been performed. However, as coverage approaches have evolved, new use models have emerged for these tools that increases their value in the verification process. The ability of coverage tools to provide guidance to areas insufficiently tested, or uncover buggy scenarios is still being explored, to great effect. Mutation coverage is a relatively new technique pioneered by formal and simulation providers. The approach is to pose the question: if my design is fully covered by a specific testbench or assertion set, then if I change something in the design, the tests should detect this change. If it doesn't then the area of change is not covered. Now if all the code segments across a block are changed, one by one, a very precise coverage metric may be established. Of course, how the design is changed, or mutated, and how these mutations are implemented has consequences on the effectiveness and performance of the solution, but the approach is widely regarded as a highly effective method for establishing both structural and functional coverage, and is used in design flows where high degrees of coverage are mandatory.

Leveraging this mutation technique with formal tools provides significant technology benefits, which accelerates the operation of the tool. In addition, the exhaustive nature of formal further improves the precision of the established coverage metric and allows for useful information on the source of uncovered scenarios to be obtained. The performance and informative nature of formal-based mutation coverage has opened up a new use model in the area of bug hunting, where the tools may be used to analyze complex operational scenarios and detect extremely well hidden error conditions, otherwise hard-to-find using more traditional solutions. This tutorial will focus on this bug hunting process. Leveraging a classic case study notorious for complex bugs, the attendees will be guided through a range of techniques applicable to many design applications, and shown how unusual bugs can manifest themselves and be detected using this technique. The workshop agenda will consist of: Introduction to mutation coverage techniques Mutation coverage with formal – it's not so tough! Sign-off with mutation coverage Overview of bug hunting techniques with formal Bug hunting using mutation coverage Bug hunting on a practical design example Overview of potential improvements using this technique.

Speaker:
Vladislav Palfy - OneSpin Solutions GmbH

Thank you to our Sponsor:
DV Tutorial 2 - How to Stay Out of the News with ISO26262-Compliant Verification

Time: 13:00 - 14:30 | Room: Ballroom A

Organizer:
Rebecca Granquist - Mentor, A Siemens Business

As the transportation industry continues to increase the amount of electronics and embedded software included in its products, systems and semiconductor makers must now consider the fault tolerance of their product offerings to customers in this rapidly growing market. Fortunately, the ISO 26262 standard defines straightforward metrics for evaluating the “safeness” of a design by defining safety goals, safety mechanisms, and fault metrics. However, even though there are sections of ISO 26262 dedicated to electronic systems in general, and semiconductors in specific, the mapping of the specification to the implementation of design and verification best practices is not specifically defined.

Hence, in this tutorial you will learn:

• What are the basics of the ISO26262 standard as it applies to requirements for electronic design & verification of safety critical products

• How to estimate the “safeness” of a design by defining safety goals, selecting “safety mechanisms”, and specifying fault metrics

• How today's dynamic, static, and hardware-assisted verification flows can be employed to verify the safety-critical RTL designs, gate-level implementations, and embedded bare-metal software and firmware

• Advanced techniques to eliminate large numbers of irrelevant faults without compromising the completeness of the verification, or the safety of the finished product

Speaker:
Charles Kuo - Mentor, A Siemens Business

Thank you to our Sponsor:

DV Tutorial 3 - Synopsys FPGA Platform – Enabling Significant Productivity Gains in Design, Verification and Debug of FPGA-based Designs

Time: 13:00 - 14:30 | Room: Ballroom B

The size and complexity of FPGA designs are getting larger with each design and designers are asked to achieve more with less. As the complexity grows, FPGA designers are under increasing pressure to accelerate designs, which has the potential cause more bug escapes. This means that FPGA designers need to segment the design flow into multiple phases to gain productivity improvements at each phase. This flow includes planning, static and formal verification, simulation synthesis and system debug, and FPGA designers need sophisticated solutions to help automate and accelerate the overall design flow with the goal of finding and fixing bugs faster with the highest performance in the smallest area.

This tutorial will detail how Synopsys solutions provide designers with industry leading tools along with native integrations, faster performance and technology advancements, to achieve the fastest time to market and highest quality FPGA designs.

Speaker:
Leon Yin - Synopsys, Inc.

Thank you to our Sponsor:
**Session 1 - Verification Methodology: Formal & Emulator**

*Time: 14:45 - 15:45 | Room: Ballroom A*

**Chair:**
Ajeetha Kumari - CVC Pvt., Ltd.
Roman Wang - Advanced Micro Device, Inc.

Verification methodology is getting more and more important when it comes to IP & SoC verification. In this session we will discuss Formal verification & Emulator methodology. The one big challenge for Formal verification is how to handle inconclusive assertion. In this session part 1, we cover the methodology and experience how to close inconclusive assertion proven. Hardware accelerator is commonly used more and more in a lot of companies. In this session part 2, we cover how to conquer complex SoC test sequences with Emulator.

1.1 Handling Inconclusive Assertions in Formal Verification

**Speaker and Authors:**
Jin Hou, Mark Eslinger, Ping Yeung, Yuxin You - Mentor, A Siemens Business

1.2 Improving Verification of High-Level Synthesis IP with Sequential Equivalency Checking

**Speaker and Authors:**
Xingri Li, Dave Pursley - Cadence Design Systems, Inc.

**Session 2 - State Based Reference Model Innovation and Dynamic Configurable Testbench in SOC**

*Time: 14:45 - 15:45 | Room: Ballroom B*

**Chair:**
Darko Tomusilovic - VTool Ltd.

In this session, we will cover IP-level Reference Modeling & Dynamic Configurable Test-Adaptive Testbench Infrastructure for SoC Verification.

2.1 A UVM-based Generic Dynamic Configurable Test-Adaptive Testbench Infrastructure for SoC Verification

**Speaker and Authors:**
Kyle Liu, Harry Huang, Gregory Brandon, Joshua Xue, Laughing Li - Advanced Micro Devices, Inc.

2.2 State Based Reference Model for Verification

**Speaker and Authors:**
ZhiGuo Liu, WenJie Meng, Min Yin - Integrated Device Technology, Inc.
Chair:
Jun Tao - Fudan Univ.

DRAM memory controllers have gained a lot of popularity in recent years. They are widely used in applications ranging from smart phones to high performance computers. These applications requires large amount of memory accessing. However, memorywall is still a bottleneck. In this session part1, we introduce the most recent techniques used to enhance DRAM Memory controllers in terms of power, capacity, latency and bandwidth. In this session part2 we cover register & memory sequence seamless reuse in IP and SoC verification.

3.1 Techniques to Enhance DRAM Memory Controllers: Industrial Experiences
Speaker and Author:
Khaled Mohamed - Mentor, A Siemens Business

3.2 Making Register and Memory Sequence Seamless Reuse in IP and SoC UVM Verification
Speaker and Author:
Roman Wang - Advanced Micro Devices, Inc.

Session 4 - Performance & Efficiency

Time: 16:00 - 17:00 | Room: Ballroom B

Chair:
Peiyu Liu - Qualcomm, Inc.

Modern SoC size and complexity grow too fast, which brings a big challenge to strive for a qualified verification through the module level to the system level. In this session, we will address the most concerned challenges in SOC level verification. such as performance monitor/analysis, functional coverage, simulation efficiency.

4.1 A Full-Scale System Monitor and Evaluation Solution for SoC Verification
Speaker and Authors:
Bin Liu, Haibo Shao - Intel Corp.
Xiuqin Zhang - Xi'an UniIC Semiconductors
Xinpan Man - Intel Corp.

4.2 An SoC Verification Methodology using a C/C++ Processor Model in the RTL Simulation
Speaker and Authors:
Lu Hao, Hong Xu - NXP Semiconductors
Poster Session

Time: 17:00 - 18:00 | Room: Foyer

Chairs:
Bin Liu - Intel Corp.
Justin Wang - MediaTek, Inc.
David Zhang - Cadence Design Systems, Inc.
Roman Wang - Advanced Micro Devices, Inc.
Leo Fang - Synopsys, Inc.
Yong Chen - Advanced Micro Devices, Inc.

5.1 A Research on the Controllability of Randomization in Verification Environment
Speaker and Authors:
Guoqing Hu, Xiaobing Zhang, Yao Zhan - MediaTek, Inc.

5.2 Coverage Driven Clock Domain Crossing Verification
Speaker and Authors:
Kurt Takara, Chris Kwok, Yuxin You - Mentor, A Siemens Business

5.3 Index based Scoreboard for SATA IP Verification Based on UVM
Speaker and Authors:
Linda Cheng, Ji Zhibin - Advanced Micro Devices, Inc.

5.4 Development of CAN Bus Protocol Controller Verification IP based on UVM
Speaker and Authors:
Zhihua Feng - Institute 706, The Second Academy China Aerospace Science & Industry Corp.
Wei Shen - Northwestern Polytechnical Univ.
Dongfang Li - Institute 706, The Second Academy China Aerospace Science & Industry Corp.
Anping He - Lanzhou University
Lirong Chen - Institute 706, Second Academy of China Aerospace and Industry Corp.
Dejun Mu - Northwestern Polytechnical Univ.

5.5 UVM Registers from the Inside Out
Speaker and Authors:
Rich Edelman, Yuxin You - Mentor, A Siemens Business

5.6 Advanced UVM Factory Use Cases
Speaker and Author:
Darko M. Tomusilovic - VTool Ltd.

5.7 A Run-time Interactive Scenario Controlling Method
Speaker and Authors:
Hong Cui, Lingyun Wu, Mengru Si - MediaTek, Inc.

5.8 Create user Adaptive and Reusable UVM Agent by Layered pcie VIP for Non-Standard PCIE Controller Verification
Speaker and Authors:
Linda Cheng, Ji Zhibin - Advanced Micro Devices, Inc.

5.9 A Practical XOR Self-Gating Method for Dynamic Power Saving
Speaker and Authors:
Chai Yihua, Yang Wang - Intel Corp.

5.10 MCERTL: Mutation-Based Correction Engine For RTL Designs
Speaker and Author:
Khaled Mohamed - Mentor, A Siemens Business

5.11 Designing a Hybrid Functional Coverage to Enhance SoC Verification
Speaker and Authors:
Peng Zhang, Zhiwen Zhang - Advanced Micro Devices, Inc.

5.12 Built a Novel Marvell Ethernet PHY Chip Verification Platform Basing on the Marvell Unique Centralized-Management Methodology/Block Architecture and the Random Stimulus Input Variable Table Idea
Speaker and Author:
Peter Wang - Marvell Semiconductor, Inc.

5.13 Automated Formal Verification of SystemC/C++ High-Level Synthesis Models
Speaker and Authors:
Sergio Marchese, Sven Beyer, Vladislav Palfy - OneSpin Solutions GmbH

5.14 Hierarchical Clock Domain Crossing Methodology for Reconvergence Closure on Complex SoCs
Speaker and Authors:
Aditya Vij - Mentor, A Siemens Business
Apoorv Aggarwal - Advanced Micro Devices, Inc.
Our industry has experienced remarkable breakthroughs in computing, networking, and communication technology in recent years. Yet, it is the convergence of these technologies that is driving the next big thing in innovation related to IoT and autonomous systems. And it is also driving the need for new approaches to verify today’s complex systems. In this keynote, Harry Foster shares a holistic view of the next big wave in verification.

**Biography:** Harry Foster is Chief Verification Scientist for the Design Verification Technology Division of Mentor, A Siemens Business; and is the Co-Founder and Executive Editor for the Verification Academy. He holds multiple patents in verification and has co-authored six books on verification. Harry was the 2006 recipient of the Accellera Technical Excellence Award for his contributions to developing industry standards, and was the original creator of the Accellera Open Verification Library (OVL) standard.
Exhibitor Listing

Visit the DVCon China 2018 Expo exhibitors in the Foyer!

Exhibit Hours:
*Wednesday, April 18: 10:00 - 18:00*

DVCon China 2018 Exhibitors

<table>
<thead>
<tr>
<th>Company Name</th>
<th>Booth Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>Arcas-tech</td>
<td>14</td>
</tr>
<tr>
<td>Blue Pearl Software</td>
<td>8</td>
</tr>
<tr>
<td>Breker Verification Systems</td>
<td>6</td>
</tr>
<tr>
<td>Cadence Design Systems, Inc.</td>
<td>2</td>
</tr>
<tr>
<td>Cloud Testing Services, Inc.</td>
<td>13</td>
</tr>
<tr>
<td>Concept Engineering GmbH</td>
<td>7</td>
</tr>
<tr>
<td>Doulos</td>
<td>15</td>
</tr>
<tr>
<td>E-Elements Technology Co., Ltd.</td>
<td>11</td>
</tr>
<tr>
<td>HyperSilicon Co., Ltd.</td>
<td>12</td>
</tr>
<tr>
<td>Mentor, A Siemens Business</td>
<td>3</td>
</tr>
<tr>
<td>OneSpin Solutions</td>
<td>4</td>
</tr>
<tr>
<td>PRO DESIGN Electronic GmbH</td>
<td>10</td>
</tr>
<tr>
<td>Real Intent, Inc.</td>
<td>9</td>
</tr>
<tr>
<td>SmartDV Technologies India Private Ltd</td>
<td>1</td>
</tr>
<tr>
<td>Synopsys, Inc.</td>
<td>5</td>
</tr>
</tbody>
</table>

Exhibitor Floorplan
Exhibitor Listing

*Exhibitors as of March 30, 2018
Arcas-tech

**Tabletop Exhibit: 14**

**www.arcas-tech.com**

Arcas Information Technology was founded in 2015 in Silicon Valley to provide new integrated circuit design automation (EDA) solutions and consulting services. The founding team has received doctorates from overseas renowned universities, including two undergraduates graduated from Tsinghua University. The founder used to be the head of R&D and management of important products of many EDA start-up companies and leading companies, with the industry's most cutting-edge core technologies. The company's first round of financing was successful this year, with R&D and marketing departments in Silicon Valley and Chengdu Hi-tech Zone.

The company currently has two products for equivalence verification and formal verification, multiple leading edge algorithm engines, multi-core, multi-machine, parallel computing, and cloud computing capabilities. In addition to product sales, we also provide training, design consulting and joint development cooperation.

Cloud Testing Services, Inc.

**Tabletop Exhibit: 13**

**www.cts-advantest.com/en**


Breker Verification Systems

**Tabletop Exhibit: 6**

**www.brekersystems.com**

Breker Verification Systems is the Portable Stimulus leader, adding GPS to your verification. Compliant with the upcoming Accellera Portable Stimulus standard, Breker automates the generation of target-specific, multi-threaded tests cases, by taking as inputs a single, executable Graph-based, Portable stimulus or spec of your verification intent, Shareable across platforms and projects.

Breker Verification Systems is the portable stimulus leader. This provides verification users with a process that provides an easy, affordable, and high-quality solution for the verification of complex systems. The system is designed to provide an intuitive and easy-to-use interface that allows users to quickly and easily create test cases for their systems.

Concept Engineering GmbH

**Tabletop Exhibit: 7**

**www.concept.de**

Concept Engineering provides visualization and debugging technology for electronic circuits and systems. The company's technology helps electronic design engineers to easily understand, debug, optimize and document electronic designs at system level, RTL level, netlist level and transistor level. Concept Engineering's software is used in many applications, including: RTL development, IP reuse, SoC design, FPGA design, analog/mixed-signal design and post-layout analysis.

Concept Engineering为电子电路和系统提供可视化和调试技术。该公司的技术帮助电子设计工程师在系统级, RTL级, 网表级和晶体管级上轻松理解，调试，优化和生成设计文档。Concept Engineering的软件可以在许多应用中使用，包括: RTL开发, IP重用, SoC设计, FPGA设计, 模拟/混合信号设计和后端布局分析。

Blue Pearl Software

**Tabletop Exhibit: 8**

**www.bluepearlsoftware.com**

Blue Pearl Software, an industry leading provider of design automation software for ASIC, FPGA and IP RTL verification, offers unparalleled ease of use with its Analyze RTL™ Linting, debug, and CDC solutions. Improving quality of results and accelerating RTL error find/fix rates while ensuring uniform coding styles, Blue Pearl provides consistent results, SDC generation and runs on Linux and Windows.

Cadence Design Systems, Inc.

**Tabletop Exhibit: 2**

**www.cadence.com**

Cadence enables electronic systems and semiconductor companies to create the innovative end products that are transforming the way people live, work and play. Cadence software, hardware and semiconductor IP are used by customers to deliver products to market faster. The company's System Design Enablement strategy helps customers develop differentiated products—from chips to boards to systems—in mobile, consumer, cloud datacenter, automotive, aerospace, IoT, industrial and other market segments. Cadence is listed as one of Fortune Magazine's 100 Best Companies to Work For.

Cadence公司致力于推动电子系统和半导体公司设计创新的终端产品, 以改变人们的工作, 生活和娱乐方式。客户采用Cadence的软件, 硬件, IP和服务, 覆盖从半导体芯片到电路板设计乃至整个系统, 帮助他们能更快速度向市场交付产品。Cadence公司创新的“系统设计实现” (SDE) 战略, 将帮助客户开发出更具差异化的产品, 无论是移动设备, 消费电子, 云计算, 汽车电子, 航空, 物联网, 工业应用等其他的应用市场。Cadence公司同时被财富杂志评选为“全球年度最适宜工作的100家公司”之一。

Concept Engineering为电子电路和系统提供可视化和调试技术。该公司的技术帮助电子设计工程师在系统级, RTL级, 网表级和晶体管级上轻松理解，调试，优化和生成设计文档。Concept Engineering的软件可以在许多应用中使用，包括: RTL开发, IP重用, SoC设计, FPGA设计, 模拟/混合信号设计和后端布局分析。
Exhibitor Listing

Doulos

Tabletop Exhibit: 15
www.doulos.com

Doulos has set the industry standard for quality training and KnowHow for over 25 years in design and verification languages and methodologies for system, hardware, and embedded software designers.

At DVCon Shanghai:
- find out about on-site team and live online training
- discover Doulos’ free online simulation environment – EDA Playground

More details: www.doulos.com

E-Elements Technology Co., Ltd.

Tabletop Exhibit: 11
www.e-elements.com

E-Elements

Founded in 2004, E-Elements initially engages in advanced FPGA (Field Programmable Gate Array) system design, training, technological consultation services, and supplying laboratory equipment of universities. The company aims at establishing long-term strategic partnership with world-leading PLD/SOC manufacturers to offer leading SOC/FPGA/ASIC design services to customers with high-tech and competitive solutions and cooperate with universities, research institutes and enterprises on new technology popularization.

Mentor, A Siemens Business

Tabletop Exhibit: 3
www.mentor.com

Mentor®, A Siemens Business delivers the most comprehensive Enterprise Verification Platform™, delivering performance and productivity improvements ranging from 400X to 10,000X. Tightly integrated combining Questa® for high performance simulation, VIP, verification management, portable stimulus, low-power, CDC & Formal Verification, Veloce® for hardware emulation and HW/SW system verification, Catapult® for High-Level Synthesis, PowerPro® for RTL Low-Power unified with the Visualizer™ debug environment.

HyperSilicon Co., Ltd.

Tabletop Exhibit: 12
www.hypersilicon.com

HyperSilicon is one of the leading suppliers of FPGA based rapid system prototype and desktop emulator for SoC design industry. We provide flexible, reliable SoC/ASIC verification platform, fastest desktop emulator and FPGA based customizing design services. With over 15 years in SoC/ASIC verification market, we have built excellent long term partnership with an impressive number of customers worldwide.

OneSpin Solutions

Tabletop Exhibit: 4
www.onespin.com

OneSpin Solutions, a leader in formal verification, is creating the industry's most advanced formal platform, encompassing agile design evaluation, coverage-driven ABV, and automated DV apps. The world's leading electronics companies partner with us to pursue design perfection in areas where reliability really counts: safety-critical verification, SystemC/C++ HLS code analysis, and FPGA equivalence checking. OneSpin: Making Electronics Reliable.
Dvcon expo
Exhibitor Listing

PRO DESIGN Electronic GmbH

**Tabletop Exhibit: 10**

www.prodesign-europe.com

PRO DESIGN is a leading provider of FPGA-based Prototyping systems. PRO DESIGN's product family proFPGA is a very flexible high-performance FPGA system which is mainly used for ASIC Prototyping and pre-silicon software development. The modular concept of the proFPGA system, consisting of different motherboards, FPGA modules, daughter boards and interconnects allows the user to adjust it for almost any type of application.

PRO DESIGN是全球领先的基于FPGA的原型验证系统方案提供商。PRO DESIGN的产品系列proFPGA提供极其灵活且高性能的FPGA系统，主要面向ASIC原型验证及流片前的软件开发。proFPGA系统采用模块化理念，由多种不同的母板、FPGA芯片、子板及互联构成，允许用户灵活调整有效应对各种不同类型的应用。

Real Intent, Inc.

**Tabletop Exhibit: 9**

www.realintent.com

Real Intent is the leading provider of EDA software to accelerate Early Functional Verification and Advanced Sign-off of digital designs. It provides comprehensive linting, clock-domain and reset crossing verification, advanced RTL analysis, and sign-off solutions to eliminate complex failure modes of SoCs. The Verix, Meridian, and Ascent product families lead the market in performance, capacity, accuracy, and completeness.

Real Intent是一家业界领先的EDA公司，致力于加速数字设计的早期功能验证和验收。公司为客户提供完整的代码风格检查、时钟域路径验证、复位域路径验证、先进的RTL分析等验收解决方案，从而为客户极大减少SoC芯片中各类复杂的失效模式。公司的Verix，Meridian，及Ascent产品系列在性能、容量、准确性和完整性方面均居市场领先地位。

SmartDV Technologies India Private Ltd.

**Tabletop Exhibit: 1**

www.smart-dv.com

SmartDV offers high quality standard and custom protocol Verification IPs, Memory Models, Simulation Acceleration IPs and Design IPs covering MIPI, Networking, Video, Storage, Automotive, SOC areas. The VIPs and IPs are licensed to 120+ customers all around the world. SmartDV also offers design and verification services in the area of ASIC and FPGA design, with emphasis on quality deliverable. SmartDV VIPs are 2-4x faster to compile and simulate compared to our competition.

SmartDV提供高品质的标准和定制协议验证IP，存储器模型，仿真加速IP和涵盖MIPI，网络，视频，存储，自动化和SOC领域的设计IP。这些VIP和IP被授权给全球120多个客户。SmartDV还提供ASIC和FPGA设计领域的设计和验证服务，重点在于可交付的质量。与我们的竞争对手相比，这些SmartDV VIP的编译和模拟速度还要快2到4倍。

Synopsys, Inc.

**Tabletop Exhibit: 5**

wwwww.synopsys.com

Synopsys is the Silicon to Software partner for innovative companies developing electronic products and software applications. Synopsys' Verification Continuum combines best-in-class technology, including simulation, verification IP, emulation, advanced debug, static and formal verification, prototyping and virtual prototyping, with advanced methodologies enabling users to address rapidly escalating SoC complexity, accelerate time-to-market and bring products to market sooner.

Synopsys致力于创新改变世界，在芯片（Silicon）到软件（Software）的众多领域，Synopsys始终引领和参与全球各个科技公司的紧密合作，共同开发人们所依赖的电子产品和软件应用。Synopsys的连续验证平台（Verification Continuum）采用一流的技术，包括仿真、验证IP、硬件加速、先进调试技术、静态和形式验证、原型和虚拟原型验证等，使用先进的方法，使用户能够解决快速升级的SoC复杂性，加快上市时间，尽快将产品推向市场.
业界运行速度最快的硬件仿真系统...
三年内销售增长最快的硬件仿真系统

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