

2019 Call for Tutorials

SUBMISSION DEADLINE: NOVEMBER 23, 2018

April 17, 2019 | Crowne Plaza Hotel Century Park, Shanghai, China

IMPORTANT DATES

- **November 23:** Tutorial submission deadline
- **December 11:** Tutorial accept/reject notification
- **January 10:** Deadline to submit final tutorial description, title, and presenter information for DVCon China website and publications
- **March 19:** Draft Presentation Slides Due to Tutorial Chair for Review
- **April 3:** Final Presentations Slides Due for Proceedings
- **April 17:** DVCon China 2019 conference

The **Design and Verification Conference & Exhibition China (DVCon China)** is a highly technical conference in China targeting the application of standardized languages, tools and methodologies for the design and verification of electronic systems, embedded systems and integrated circuits. Hosted by Accellera Systems Initiative, the format of DVCon China is similar to the successful DVCon United States conference held for over 10 years in the Silicon Valley.

The ultimate goal of DVCon China is to boost the interest, usage and development of electronic system designs. DVCon China is looking for tutorial topics that are current, have a high-level of interest and offer strong continuing educational content. Highly qualified engineers are expected to attend the sponsored tutorials during DVCon China 2019. Tutorial sponsorship allows companies to reach a captive audience during the half-day educational sessions and the opportunity to follow up with them during breaks, at the exhibits, and following the event. DVCon China is a highly targeted venue for engineers addressing major design and verification issues. You can position your company at the forefront of these discussions by sponsoring a tutorial. Unlike other conferences, there is no extra charge for attending the tutorials. The presenter is virtually guaranteed a good attendance. Few topics are:

- Modeling, Design and Verification of complex electronic systems at different levels of abstraction such as Virtual prototyping, Architectural Modeling, RTL, Emulation, HW acceleration, etc.
- The application of system-level design and verification languages such as SystemC, SystemVerilog
- Virtual Platform for Embedded Software Development
- SoC Design Verification using the latest trends and methodologies such as UVM-SystemC, graph-based techniques, portable stimulus across block-subsystem-system all the way up to Post-Silicon
- The use of SystemVerilog Assertions (SVA), PSL and Formal Verification (Model Checking)
- Adoption of Universal Verification Methodology (UVM)
- IP reuse, design automation and integration standards based on IP-XACT, SystemRDL
- Low-power design and verification using the Unified Power Format (UPF)

General topic areas on Electronic System Level (ESL), Virtual Platform, Verification & Validation, Analog/Mixed-Signal, IP reuse, Design Automation, and Low-power design and verification will be highlighted in tutorials, papers, and poster sessions.

Conference attendees are primarily designers of embedded systems, electronic systems, ASICs and FPGAs, as well as those involved in the research, development and application of EDA tools and IP integration solutions. The DVCon China conference attracts a highly skilled user base active in various industries focusing on research and development of automotive, aerospace, consumer, and wired and wireless communication products.

2019 CALL FOR TUTORIALS — ESL TRACK

DVCon China solicits detailed proposals for tutorials that are highly technical and reflect real life experiences in using languages, standards, methods and Electronic Design Automation (EDA) tools.

The ESL track aims to accelerate the adoption of SystemC in the Semiconductor Industry. It provides a platform for the SystemC beginners, SystemC/TLM experts, ESL managers and ESL vendors to share their knowledge, experiences & best practices about SystemC usage. Submissions are encouraged in (but not restricted to) the following topics:

- Virtual-Platforms and System-Level Design
 - Transaction-level modeling for system-level design
 - Hardware/software/embedded co-design
 - System-level design techniques, flows and methodologies
 - High-level synthesis from ESL languages
- Power
 - Low Power Design
 - Power estimation techniques
 - Power modeling
- Mixed-Signal (AMS)
 - SystemC AMS usage for mixed-signal simulation
 - AMS system-level and concept design

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2019 CALL FOR TUTORIALS — DV TRACK

In the DV Track we are soliciting detailed proposals for tutorials from industry leaders in the field of Design & Verification. The DV Track provides a platform for the wide Design-Verification community including beginners, intermediate and seniors to learn the latest concepts, techniques, etc. in their respective domains of interest. Submissions are encouraged in (but not restricted to) the following topics:

- UVM – Universal Verification Methodology
- Latest language developments in SystemVerilog including:
 - New and enhanced constructs
 - Assertion enhancements
- Advanced stimulus generation methods, reuse of stimulus across levels of verification (Portable Stimulus)
- Formal Verification
 - Coding styles, techniques for assertions for formal
 - Model Checking techniques, target designs/blocks
- Compliance and Requirements-driven verification such as DO-254 and ISO 26262 standards
- Debug automation through transaction-level debug, smart tricks to handle performance issues, faster time to debug techniques
- Low Power intent verification through standards such as UPF and related technologies
- Use of IPXACT, SystemRDL in design flow
- Digital and Analog Mixed Signal (AMS) techniques
- Emulation, Acceleration, Prototyping

TUTORIAL SUBMISSION PROCESS

Tutorials are 120-minute sessions. DVCon China attendees have the opportunity to learn about different topics during the sessions. A tutorial may have a single speaker or several speakers. In either case, the submitter is responsible for organizing the tutorial. Multiple companies can join together to sponsor a tutorial.

If you are interested in providing a tutorial session, please submit your abstract by **November 23** and indicate that this is a tutorial submission. By submitting the tutorial proposal, you agree to become the tutorial sponsor.

SPONSORED TUTORIAL: RMB 19,570

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This opportunity includes:

- A 1.5 hour technical tutorial prepared and presented by your company
- Your company logo will be displayed on the event venue (stage backdrop)
- Your company logo will be displayed on the conference website
- Includes 2 free registrations for speakers
- Your company mentioned in the Opening Session

Note: Tutorials will be reviewed and approved by the program committee with respect to technical depth and applicability. In case of multiple organizations coming together for a tutorial only 1 organization would get the sponsorship benefits mentioned above.

A tutorial abstract is expected to include the following details:

- Abstract title stating that this is a tutorial submission
- Name, affiliation, phone number and email addresses for all speakers
- An introduction that specifies the context and motivation of the tutorial submission (MAX 1000 words)
- A summary of the specific content of your tutorial and your intended audience. For each presentation, mention the title and a short paragraph description.
- Must be descriptive enough to see what this tutorial will address and what the attendees would learn from it
- Maximum 3 pages

There is no template for the proposal.

- Provide enough details so that the Technical Program Committee can evaluate the potential quality and interest of your possible tutorial at DVCon China 2019.
- Please submit your proposal by **November 23**.



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TUTORIAL ROLES

Tutorial Organizer: For the selected tutorial, the Organizer coordinates all tutorial activities with DVCon China, including ensuring that content is delivered in a timely manner and that the final presentation goes smoothly; follow-through is critical, the Organizer must interact with the Conference Coordinator (contact: Jackie McIntosh at jackie@mpassociates.com).

- The Organizer writes the proposal for the tutorial and the abstract that is submitted for proposal evaluation.
- The Organizer selects and confirms the participation of the Presenter(s) (who could include the Organizer).
- The Organizer writes the material that will be included in the website and publications. It is very important that the Organizer write the material to help a potential attendee decide if they should attend this tutorial.
- The program material should describe the target audience and their expected level of familiarity with the topic (Expert/Intermediate/Beginner).
- An Organizer can propose multiple tutorials on aligned topics with different speakers.

Presenter: The Presenter is responsible for delivering the presentation.

Questions?

Feel free to contact Jackie McIntosh at jackie@mpassociates.com for questions on the submission process.

DVCon China reserves the right to restructure all tutorial suggestions.