2019 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION CHINA

Call for Short Workshops

April 17, 2019 | Crowne Plaza Hotel Century Park, Shanghai, China

DVCon China is the premier conference on the application of languages, tools, and methodologies for the design and verification of electronic systems and integrated circuits. The focus of the conference is the usage of specialized design and verification languages such as Verilog, SystemVerilog, VHDL, PSL, SystemC and e, as well as general purpose languages such as C, C++, PERL, Tcl, and Python. Tools and methodologies include the use of testbench automation, portable stimulus, hardware-assisted verification, hardware/software co-verification, assertion-based and formal verification, transaction-level system design, high level synthesis, low power design techniques, 3D chip designs, IP based SoC design methods, reference flows and AMS design.

DVCon China is looking for short workshops to encourage greater sponsorship participation from companies and exhibitors, especially smaller organizations at an affordable level.

DVCon China is looking for short workshop topics that are current, have a high-level of interest and offer strong continuing educational content.

Short Workshop sponsors reach a captive audience during the 60-minute educational sessions and have the opportunity to follow-up with attendees during breaks, at the exhibits, and following the event.

DVCon is a highly-targeted venue for engineers addressing major design and verification issues. Submit proposals by **November 23, 2018**

DVCON CHINA SPONSORED SHORT WORKSHOP: RMB 6,500

Sponsorship Includes:

- A 45 minute Short Workshop presentation
- Short Workshop content will be publicized via monthly newsletters, DVCon website, Conference Program and in the Opening Session
- One dedicated email distribution to the DVCon mail list
- Other promotion items like banners, flyers, gift items, etc may be distributed during the Short Workshop

For more information concerning the conference, please contact the conference management, Jackie McIntosh at jackie@mpassociates.com

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SHORT WORKSHOP PROPOSAL REQUIREMENTS

Deadline: November 23, 2018

- Please include in the proposal the name of the companies that will be sponsoring the short workshop.
- Include suggested presenters names, affiliations and biographies.
- Your proposal should be a short abstract of the short workshop, two to five paragraphs, 1,000 words maximum
- Please indicate if this short workshop is a "hands-on" session or lecture format
- Any necessary additional hardware that you may require must be provided by the short workshop organizers

SUGGESTED TOPICS

- SystemVerilog for Verification and/or Design
- SystemC /C/C++ Design and/or Verification of systems.
- SoC and Software-driven Verification
- Assertion-based Verification. SystemVerilog Assertions, PSL, etc.
- Coverage-driven Verification
- High-level Synthesis
- Low-power Design and Verification techniques
- Secure/Encrypted IP-based SoC design methods
- Debug for design and verification
- Mixed-signal modeling and verification
- Transaction Level Modeling (TLM), ESL Design, and IP integration (IP-XACT)
- Functional Safety
- Security
- Embedded software verification
- Hardware/Software Co-development
- Verification Productivity Methods
- Formal Methodology and Static Analysis
- Emulation
- Post SI Debug
- FPGA Prototyping
- Moving from proprietary solutions to standards-based design and verification
- Portable Stimulus
- Application based design verification challenges, techniques

SHORT WORKSHOP DEADLINES

November 23, 2018:	Short Workshop Proposal Due
December 11, 2018:	Accept/Reject Notification
January 10, 2019:	All Short Workshop content due for Conference Program and website: title, abstract, speaker names, affiliations and biographies
March 19, 2019:	Draft Presentation slides due to DVCon Tutorial Chair
April 3, 2019:	Final slides due for final production for attendee distribution

SPONSORED BY: Accellera Systems Initiative is an industry consortium with a mission to provide design and verification standards required by systems, semiconductor, IP, and design tool companies to enhance a front-end design automation process. **Accellera.org**

Conference Sponsor:

accellera SYSTEMS INITIATIVE™

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