

# Call for Abstracts

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## 2018 Call for Abstracts

The Design and Verification Conference & Exhibition China (DVCon China) is a highly technical conference in China targeting the application of standardized languages, tools, and methodologies for the design and verification of electronic systems, embedded systems and integrated circuits.

The DVCon China 2018 cover hot topics in ASIC design and verification industry. The topics are listed in below table but are not limited to it.

### Topic Area 1: System-Level Design

- Requirements-driven design incl. traceability
- Virtual and hardware-assisted prototyping
- Architecture exploration
- Hardware/software/embedded co-design
- System-on-chip and network-on-chip design
- System development methodologies and flows
- High-level synthesis from ESL languages
- Safety and security in system-level design
- Automatic Assertion Generation
- Prototyping and Virtual Prototyping

### Topic Area 2: Verification & Validation

- Requirements-driven verification incl. traceability
- Verification process, re-use, and resource management
- Methods bridging between verification and validation
- Hardware/software co-verification
- Advanced methodologies, testbenches, and flows (e.g., UVM, HDLs, HVLs, testbench automation)
- Testbench qualification
- Formal and semi-formal techniques
- Safety and security in verification and validation
- FPGA verification and reuse
- DfX methodology

### Topic Area 3: IP Reuse and Design Automation

- Interoperability of models and/or tools
- IP tagging, protection or security
- SoC and IP integration methods, flows, and tools
- Configuration management of IPs including different abstraction levels
- Flow and tool automation (e.g., IP-XACT)



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## Topic Area 4: Mixed-Signal Design and Verification

- AMS concept and system design
- Application of mixed-signal extensions (e.g., UVM)
- Real-number modeling approaches
- Mixed-signal design and verification techniques (applied on proper abstraction level)
- Self-checking in analog verification

## Topic Area 5: Low Power Design and Verification

- Low-power design and verification challenge
- Debug methodology in low-power
- Power aware simulation
- Static Low Power Checks
- RTL Power Estimation and Optimization

## Topic Area 6: High performance design and verification

- High performance design methodology
- Performance measurement and verification
- High performance SoC Emulation

## Submission Guidelines

To spare you the many hours of preparation associated with other paper submissions, DVCon China has the following process:

- Submit a 500-1000 word abstract highlighting what you wish to present at DVCon China. The program committee will evaluate your abstract. **The deadline for abstract submission is Monday, October 9, 2017.**
- Authors of exceptionally strong abstracts will be shortlisted for oral or poster presentation at the conference.
- Consistent with the requirements for other DVCon presentations, your presentation may contain your company logo only on the title slide.

An abstract is expected to include the following details:

- A title
- Name, affiliation, phone number and email addresses for all authors.
- An introduction that specifies the context and motivation of the submission.
- A summary of the specific contributions of your work.
- A summary that highlights results. To evaluate your contribution, you must specify some results.
- References, if appropriate

Your abstract can be at most two pages. You can format it in single column format. Provide enough details so that the Technical Program Committee can evaluate the potential quality and interest of your possible presentation at DVCon China. A one-paragraph summary will not fulfill this requirement.

## Important Deadlines

- **October 9, 2017:** Abstract Submission deadline
- **December 5, 2017:** Accept/Reject notification
- **December 21, 2017:** Draft Paper Due for Review
- **February 27, 2018:** Final Paper and Copyright Form Due
- **March 13, 2018:** Draft Presentation Slides Due for Review
- **April 5, 2018:** Final Presentation Slides Due

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